


MANUFACTURE OF SEMICONDUCTOR DEVICE

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Abstract

PURPOSE: To obtain a high-frequency and high-speed vertical type PNP transistor by forming a flat low-doped collector area by suppressing the creeping-up of a buried collector layer to an epitaxial layer side by performing diffusion heat treatment, etc., after continuously performing ion implantation two or more times into the epitaxial layer with different acceleration energy.

CONSTITUTION: After a buried area 5 is formed on a semiconductor substrate 1 through a photolithographic process, an epitaxial layer 3 is formed on the entire surface of the substrate 1 and a resist 2c is formed on the layer 3 through its oxide film 4. Then an opening is formed by removing the resist 2c and film 4 on the part of layer 3 proposed to a low-doped collector layer 6a and ions are continuously implanted into the opening two or more times with different acceleration energy and diffusion heat treatment is performed. For example, boron ions are implanted by changing the acceleration energy from 500KeV to 50KeV through 300KeV, 150KeV, and 100KeV.

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